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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/773,754	02/02/2001	Ming-Dou Ker	H000039	6902

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EXAMINER
SEFER, AHMED N

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 01/15/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/773,754	KER ET AL.	
	Examiner	Art Unit	
	A. Sefer	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 October 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 10/31/02 has been entered.

Specification

2. The disclosure is objected to because of the following informalities: The limitation "a second region of he second ..." recited in claim 4 should read "a second region of the second ..." Appropriate correction is required.

Allowable Subject Matter

3. The indicated allowability of claims 2, 4, 7, 9, 11 and 14-19 are withdrawn in view of the newly discovered reference(s) to Hirata US Patent No. 6,469,354 and Hsu et al. US Patent No. 6,057,579. Rejections based on the newly cited reference(s) follow.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in-
(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

5. Claims 1 and 3 are rejected under 35 U.S.C. 102(e) as being anticipated by Hirata US Patent No. 6,469,354.

Hirata disclosess in figs. 5, 7 and 12 a semiconductor structure for electrostatic discharge (ESD) protection of a metal-oxide semiconductor (MOS) integrated circuit comprising a substrate of a first conductivity type forming a base for said semiconductor structure; a first region 14n of a second conductivity type within said substrate for forming a drain of a first MOS transistor; a second region 16n of the second conductivity type within said substrate for forming a source of the first MOS transistor; a third region of the second conductivity type 16n for forming a source of a second MOS transistor, wherein a fourth region 10b/26 of the first conductivity type is disposed between the second region of said first MOS transistor and the third region of said second MOS transistor for surrounding said first MOS transistor with an additional pick-up diffusion to restrain a turn-on of said first MOS transistor.

Regarding claim 3, Hirata disclosess a pre-buffer circuit coupled to a gate of the first MOS transistor; and an outpad 22 coupled to said first region of the first MOS transistor.

6. Claim 2 is rejected under 35 U.S.C. 102(e) as being anticipated by Hsu et al. US Patent No. 6,057,579.

Hsu et al disclose (see figs. 4 and 5, col. 4, lines 19-34 and claims 5 and 6) a semiconductor structure for electrostatic discharge (ESD) protection of a metal-oxide semiconductor (MOS) integrated circuit comprising a substrate of a first conductivity type forming a base for said semiconductor structure; a first region 412 of a second conductivity type within said substrate for forming a drain of a first MOS transistor; a second region 408 of the second conductivity type within said substrate for forming a source of the first MOS transistor; a third region 408 of the second conductivity type region for forming a source of a second MOS transistor, wherein a fourth region 418 of the first conductivity type is disposed between the second region of said first MOS transistor and the third region of said second MOS transistor for surrounding said first MOS transistor with an additional pick-up diffusion to restrain a turn-on of said first MOS transistor, and wherein the channel length of said first MOS transistor is longer than the channel length of said second MOS transistor to increase the drain-base voltage of said first MOS transistor.

7. Claim 4 is rejected under 35 U.S.C. 102(e) as being anticipated by Hsu et al. US Patent No. 6,057,579.

Hsu et al disclose (see figs. 4 and 5, col. 4, lines 19-34 and claims 5 and 6) a semiconductor structure for electrostatic discharge (ESD) protection of a metal-oxide semiconductor (MOS) integrated circuit comprising a substrate of a first conductivity type forming a base for said semiconductor structure; a first region 412 of a second

conductivity type within said substrate for forming a drain of a first MOS transistor; a second region 408 of the second conductivity type within said substrate for forming a source of the first MOS transistor; a third region 408 of the second conductivity type within said substrate for forming a source of a second MOS transistor, wherein a fourth region 418 of the first conductivity type is disposed between the second region of said first MOS transistor and the third region of said second MOS transistor for surrounding said first MOS transistor with an additional pick-up diffusion to restrain a turn-on of said first MOS transistor, a first channel region disposed between said first and second regions of said first MOS transistor; and a second channel region disposed adjacent to said third region of said second MOS transistor, wherein said first channel length of said first channel region is longer than the channel length of said second channel region to increase the drain-base breakdown voltage of said first MOS transistor.

8. Claim 5 is rejected under 35 U.S.C. 102(e) as being anticipated by Hsu et al. US Patent No. 6,057,579.

Hsu et al disclose (see figs. 4 and 5, col. 4, lines 19-34) a semiconductor structure for electrostatic discharge (ESD) protection of a metal-oxide semiconductor (MOS) integrated circuit comprising a substrate of a first conductivity type forming a base for said semiconductor structure; a pair of first regions 408/412 of a second conductivity type within said substrate for defining a first channel region 428 of the second conductivity type for a first MOS transistor; and a pair of second regions 412/410 of a second conductivity type within said substrate for defining a second channel region 428 of the second conductivity type for a second MOS transistor,

wherein the channel length of said first channel region is greater than the channel length of said second channel region to reduce a turn-on speed of said first MOS transistor.

9. Claim 7 is rejected under 35 U.S.C. 102(e) as being anticipated by Hsu et al. US Patent No. 6,057,579.

Hsu et al disclose (see figs. 4 and 5, col. 4, lines 19-34) a semiconductor structure for electrostatic discharge (ESD) protection of a metal-oxide semiconductor (MOS) integrated circuit comprising a substrate of a first conductivity type forming a base for said semiconductor structure; a pair of first regions 408/412 of a second conductivity type within said substrate for defining a first channel region 428 of the second conductivity type for a first MOS transistor; a pair of second regions 412/410 of the second conductivity type within said substrate for defining a second channel region 428 of the second conductivity type for a second MOS transistor, wherein the channel length of said first channel region is greater than the channel length of said second channel region to reduce a turn-on speed of said first MOS transistor; and a third region 418 of the first conductivity type between the source side of said first regions and the source side of said second regions for surrounding said first MOS transistor with an additional pick-up diffusion to further restrain the turn-on speed of said first MOS transistor.

10. Claims 8 and 10 are rejected under 35 U.S.C. 102(e) as being anticipated by Hirata US Patent No. 6,469,354.

Hirata disclosess in fig. 5, 7 and 12 a semiconductor structure for electrostatic discharge (ESD) protection of a metal-oxide semiconductor (MOS) integrated circuit comprising a p-type substrate of forming a base for said semiconductor structure; a first N+ region 14n within said substrate for forming a drain of a first MOS transistor; a second N+ region 16n within said substrate for forming a source of the first MOS transistor; a third N+ region 16n within said substrate for forming a source of a second MOS transistor, wherein a P+ region 10b is disposed between the second N+ region of said first MOS transistor and the third N+ region of the second MOS transistor for surrounding said first MOS transistor with an additional pick-up diffusion to restrain a turn-on of said first MOS transistor.

Regarding claim 10, Hirata disclosess a pre-buffer circuit coupled to a gate of the first MOS transistor; and an outpad 22 coupled to said first region of the first MOS transistor.

11. Claims 15 and 16 are rejected under 35 U.S.C. 102(e) as being anticipated by Hsu et al.

Hsu et al disclose (see figs. 1-5, col. 4, lines 19-34 and claims 5 and 6) a semiconductor structure for electrostatic discharge (ESD) protection of a metal-oxide semiconductor (MOS) integrated circuit, said semiconductor structure connected between an input pad and an internal circuit of said integrated circuit comprising a substrate of a first conductivity forming a base for said semiconductor structure; a first channel 428 formed between a pair of first regions 408, 412 of a second conductivity type within said substrate for a first MOS transistor; and a second channel 428 formed

between a pair of second regions 412, 410 of a second conductivity type within said substrate for a second MOS transistor, wherein an additional pick-up diffusion region is disposed between the source region of said first regions and the source region of said second regions for surrounding said first MOS transistor with an additional pick-up diffusion to restrain the turn-on of said first MOS transistor.

Regarding claim 16, Hsu et al disclose a channel length of said first channel longer than the channel length of said second channel to increase a drain-base breakdown voltage of said first MOS transistor.

12. Claims 17 and 18 are rejected under 35 U.S.C. 102(e) as being anticipated by Hsu et al.

Hsu et al disclose (see figs. 1-5, col. 4, lines 19-34 and claims 5 and 6) a semiconductor structure for electrostatic discharge (ESD) protection of a high-voltage tolerant I/O cells with stacked NMOS or PMOS integrated circuits, said semiconductor structure connected between a pre-driver circuit and input/output pad of said integrated circuit and comprising a substrate of first conductivity forming a base for said semiconductor structure; a first channel 428 formed between a pair of first regions 408, 412 of a second conductivity type within said substrate for a first MOS transistor which is stacked on a third MOSFET of a second conductivity type; and a second channel 428 formed between a pair of second regions 412, 410 of a second conductivity type within said substrate for a second MOS transistor which is stacked on a fourth MOSFET of a second conductivity type, wherein an additional pick-up diffusion region is disposed between the source region of said first regions and the source region of said second

regions for surrounding said first MOS transistor with an additional pick-up diffusion to restrain the turn-on of said first MOS transistor.

Regarding claim 18, Hsu et al disclose a channel length of said first channel longer than the channel length of said second channel to increase a drain-base breakdown voltage of said first MOS transistor.

13. Claim 19 is rejected under 35 U.S.C. 102(e) as being anticipated by Hsu et al.

Hsu et al disclose a semiconductor structure for electrostatic discharge (ESD) protection comprising at least one ESD protection device; and at least one guarded device which is turned –on by a turn-on restrained means, wherein the ESD protection device can be turned-on before the turn-on restrained means is turned on.

Claim Rejections - 35 USC § 103

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

15. Claims 3 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsu et al. in view of admitted prior art (APA).

Hsu et al disclose all the claimed subject matter but fail to disclose a pre-puffer circuit coupled to a channel and an output pad coupled to a first region or regions of a MOS transistor.

The APA disclose in figs. 2-5 a pre-puffer coupled to a gate of a MOS transistor or to a channel; and an output pad coupled to a region or regions of a MOS transistor.

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to incorporate the teachings of the APA with Hsu et al, since that would reduce transient contributions to a response.

16. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hirata in view of Hsu et al.

Hirata discloses (see figs. 4 and 5, col. 4, lines 19-34) a semiconductor structure for electrostatic discharge (ESD) protection of a metal-oxide semiconductor (MOS) integrated circuit comprising a p-type substrate of forming a base for said semiconductor structure; a first N+ region 14n within said substrate for forming a drain of a first MOS transistor; a second N+ region 16n within said substrate for forming a source of the first MOS transistor; a third N+ region 16n for forming a source of a second MOS transistor, wherein a P+ region 10b/26 disposed between the second N+ region of said first MOS transistor and the third N+ region of said second MOS transistor for surrounding said first MOS transistor with an additional pick-up diffusion to restrain a turn-on of said first MOS transistor, but omits a channel length of a first MOS transistor longer than a channel length of a second MOS transistor.

Hsu et al teach a channel length of a first MOS transistor longer than a second MOS transistor to increase a drain-base breakdown voltage of said first MOS transistor.

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to incorporate the teachings of Hsu et al with Hirata's device, since a longer channel length would result in slower conduction rate.

17. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hirata in view of Hsu et al.

Hirata discloses (see figs. 4 and 5, col. 4, lines 19-34) a semiconductor structure for electrostatic discharge (ESD) protection of a metal-oxide semiconductor (MOS) integrated circuit comprising a p-type substrate of forming a base for said semiconductor structure; a first N+ region 14n within said substrate for forming a drain of a first MOS transistor; a second N+ region 16n within said substrate for forming a source of the first MOS transistor; a third N+ region 16n for forming a source of a second MOS transistor, wherein a P+ region 10b/26 disposed between the second N+ region of said first MOS transistor and the third N+ region of said second MOS transistor for surrounding said first MOS transistor with an additional pick-up diffusion to restrain a turn-on of said first MOS transistor, a first n-channel region having a first channel length disposed between the first and second regions of said first MOS transistor; and a second channel region having a second channel length disposed adjacent to said third region of said second MOS transistor, but omits a channel length of a first MOS transistor longer than a second MOS transistor.

Hsu et al teach a channel length of a first MOS transistor longer than a second MOS transistor to increase a drain-base breakdown voltage of said first MOS transistor.

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to incorporate the teachings of Hsu et al with Hirata's device, since a longer channel length would result in slower conduction rate.

18. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hirata in view of Hsu et al.

Hirata discloses (see figs. 4 and 5, col. 4, lines 19-34) a semiconductor structure for electrostatic discharge (ESD) protection of a metal-oxide semiconductor (MOS) integrated circuit comprising a p-type substrate forming a base for said semiconductor structure; a pair of first N+ regions 14n, 16n within said substrate for defining a first n-channel region for a first MOS transistor; and a pair of second N+ regions 14n, 16n within said substrate for defining a second n-channel region for a second MOS transistor, but omits a channel length of a first MOS transistor longer than a second MOS transistor.

Hsu et al teach a channel length of a first MOS transistor longer than a second MOS transistor to increase a drain-base breakdown voltage of said first MOS transistor.

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to incorporate the teachings of Hsu et al with Hirata's device, since a longer channel length would result in slower conduction rate.

Regarding claim 13, Hirata disclosess a pre-buffer circuit coupled to a first channel; and an outpad 22 coupled to one of said pair of first N+ regions and one of said pair of second N+ regions.

19. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hirata in view of Hsu et al.

Hirata discloses (see figs. 4 and 5, col. 4, lines 19-34) a semiconductor structure for electrostatic discharge (ESD) protection of a metal-oxide semiconductor (MOS) integrated circuit comprising a p-type substrate forming a base for said semiconductor structure; a pair of first N+ regions 14n, 16n within said substrate for defining a first n-channel region for a first MOS transistor; and a pair of second N+ regions 14n, 16n within said substrate for defining a second n-channel region for a second MOS transistor, but omits a channel length of a first MOS transistor longer than a second MOS transistor; a third P+ region between the source region of said first N+ regions and the source region of said second N+ regions for surrounding said first MOS transistor with an additional pick-up diffusion to further restrain the turn-on of said first MOS transistor, but omits a channel length of a first MOS transistor greater than a channel length of a second MOS transistor.

Hsu et al teach a channel length of a first MOS transistor longer than a second MOS transistor to increase a drain-base breakdown voltage of said first MOS transistor.

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to incorporate the teachings of Hsu et al with Hirata's device, since a longer channel length would result in slower conduction rate.

Conclusion

20. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Avery US ref. 5,043,782 discloses an ESD protection device having a longer channel length, which conducts before a transient exceeds the breakdown voltage of an IC and a short channel length structure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to A. Sefer whose telephone number is (703) 605-1227.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on (703) 308-6601.

ANS
January 5, 2003

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